CK100 Clock Buffer
Preliminary EMI Layout Guideline

Rev. 0.51
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Scope:

This document describes an example of a layout for reducing emissions from a CK100 SDRAM Clock Buffer motherboard design.

Background:

The CK100 Buffer Part (CKBUF) takes an output clock from the Chipset and makes 18 copies for the provision of clock signals to SDRAM DIMMs. These output clocks are synchronized by definition.

Unless the outlined design guidelines are followed there is a high risk of excessive EMI problems at the higher clock harmonics.

Specifics:

Figure 1 (overleaf) illustrates one example of a PCB layout that has been shown to reduce system EMI levels related to the CK100 Buffer Part and its associated SDRAM Clock Output traces.

The critical aspects are:

Dedicated Power and Ground Planes for Clock Buffer (CK_VCC and CK_GND).

These planes should be 'cut out' planes on the normal VCC and GND layers of the PCB (Figure 2).

CK_VCC and CK_GND are connected to MB_GND and MB_VCC through low value ferrite beads (5 Ohms @ 100MHz). These beads should span the void area created by the plane split.

The motherboard layout should include provision for about 14 beads (7 on VCC, 7 on GND. This includes beads for the IIC VCC and IIC GND). The minimum number of beads should be populated while still maintaining the required rise time at the DIMMs (1V/nS).

Decoupling Capacitors between CK_VCC and CK_GND (in the order of 6 1000pF) should be placed over the CK_VCC and CK_GND "wings".

The Output Clock traces to the DIMMs should not, under any circumstances cross over any of the void areas created by the CK_VCC and CK_GND planes. These traces must have a complete plane (VCC or GND) under their entire routing length.

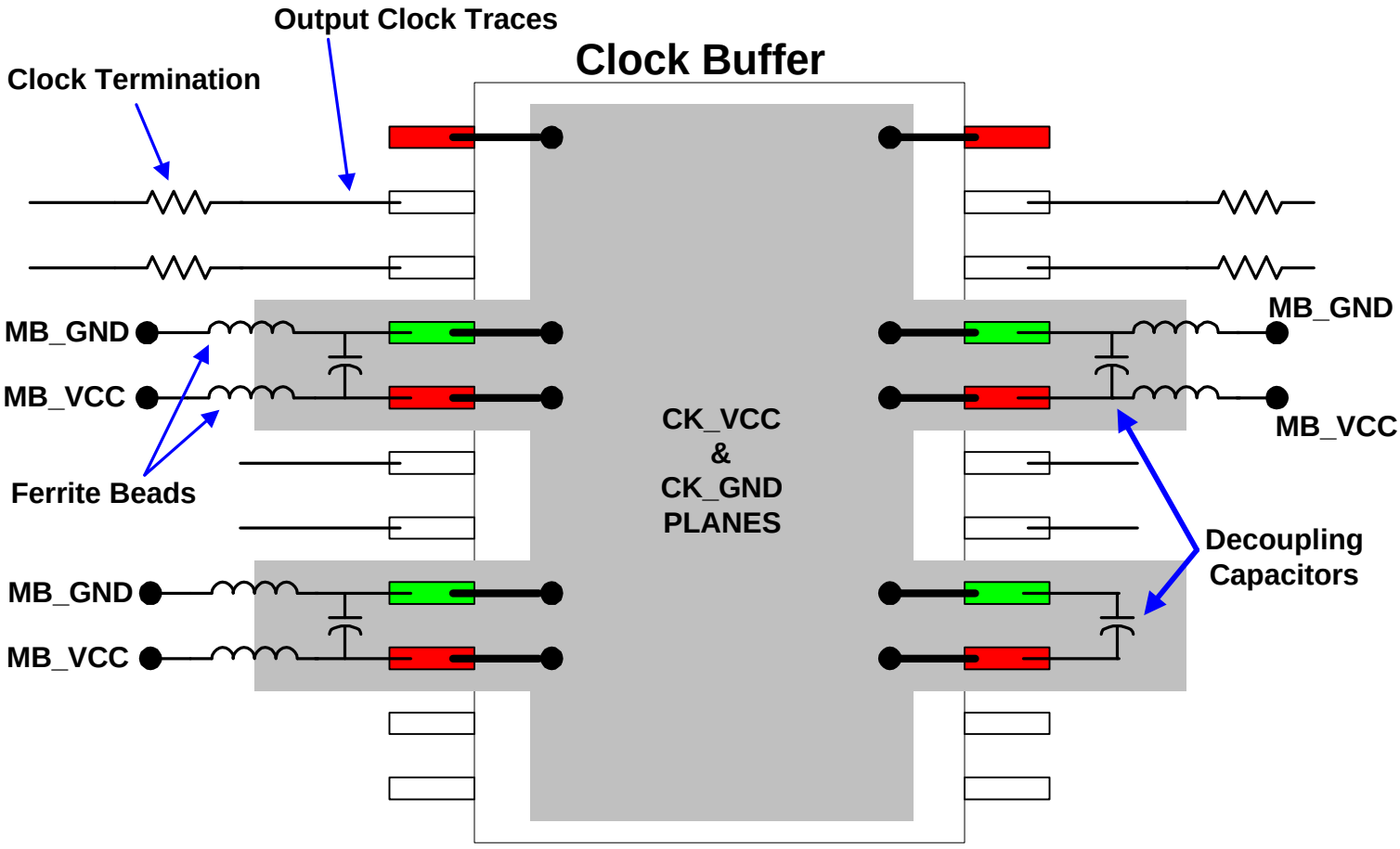

Figure 1

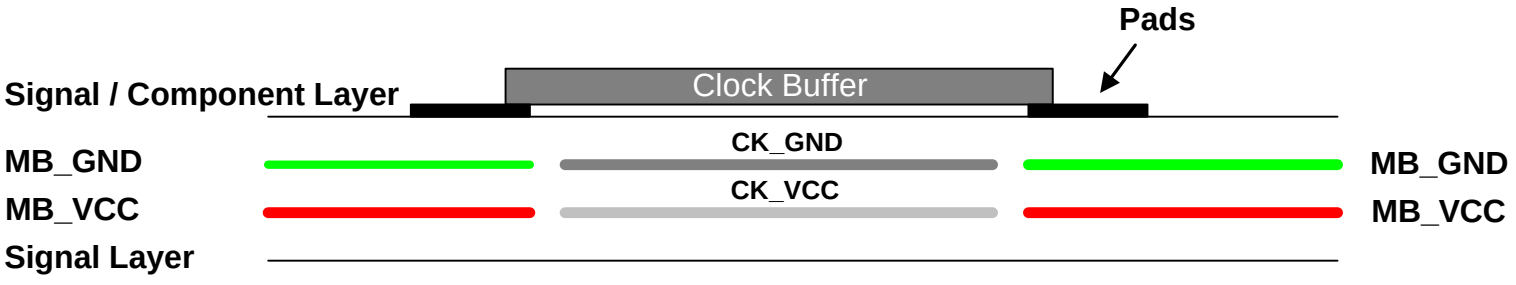

Figure 2